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Deep Etching of Single- and Polycrystalline Silicon with High Speed, High Aspect Ratio, High Uniformity, and 3D Complexity by Electric Bias-Attenuated Metal-Assisted Chemical Etching (EMaCE)

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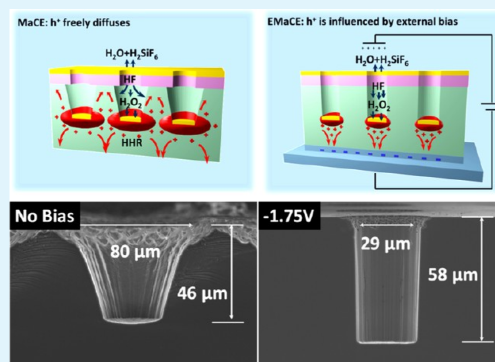
Supporting Information

ABSTRACT: In this work, a novel wet silicon (Si) etching method, electric bias-attenuated metal-assisted chemical etching (EMaCE), is demonstrated to be readily available for three-dimensional (3D) electronic integration, microelectromechinal systems, and a broad range of 3D electronic components with low cost. On the basis of the traditional metal-assisted chemical etching process, an electric bias was applied to the Si substrate in EMaCE. The 3D geometry of the etching profile was effectively controlled by the bias in a real-time manner. The reported method successfully fabricated an array of over 10 000 vertical holes with diameters of 28 μm on 1 cm^2 silicon chips at a rate of up to 11 μm/min. The sidewall roughness was kept below 50 nm, and a high aspect ratio of over 10:1 was achieved. The 3D geometry could be attenuated by the variable applied bias in real time. Vertical deep etching was realized on (100)-, (111)-Si, and polycrystalline Si substrates. Complex features with lateral dimensions of 0.8−500 μm were also fabricated with submicron accuracy.

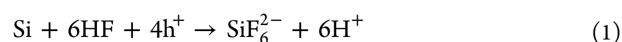


KEYWORDS: *wet etching, electrical bias, 3D microstructures*

■ INTRODUCTION

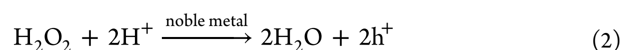
Fabrication of three-dimensional (3D) microstructures on elemental silicon (Si) is a fundamental process in manufacturing of a broad range of components in modern microelectronic devices, such as through silicon vias,[1] microelectromechanical systems,[2] optoelectronic devices[3] and etc.[4,5] Compared to the components that spread on the two-dimensional (2D) surface of Si, the 3D components utilized the volume inside Si substrates, thus gained much higher integration density and unique functions. Currently, the 3D components are majorly fabricated by bulk micromachining of Si (BMS), where a certain volume of Si inside the wafers or chips was selectively removed by wet solution (wet etching) or plasma (dry etching). However, both methods have significant limitations. Wet etching generally possesses the nature of cost efficiency, but the shape of the etching profiles is limited because the etching direction depends on the crystalline orientation of the substrate. Dry etching is virtually capable of etching microstructures with arbitrary geometry.[6,7] However, its application in large-scale manufacturing has been hindered by expensive instrumentation and maintenance. In this work, we present a novel wet BMS technology that successfully fabricated vertical holes and trenches with high aspect ratio, high uniformity, high speed, high pattern density, submicron precision, 3D geometric complexity, and low cost.

It has long been known that Si can be etched in hydrofluoric acid (HF) solution with the presence of electronic holes (h^+):



$$Si + 6HF + 4h^+ \rightarrow SiF_6^{2-} + 6H^+ \quad (1)$$

Holes (h^+) can be either generated by reduction of oxidative chemicals (for example, HNO_3) or injected from external electric power supply, as in the cases in isotropic wet etching[8] or electrochemical etching,[9,10] respectively. Because the etching of Si by pure HF is extremely slow,[11] selective etching of Si in a HF-h^+ system can be realized by controlling the distribution of h^+ concentration inside the Si substrate. Recently, a novel HF-based etching method, metal-assisted chemical etching (MaCE), has received extensive attention.[12−17] In MaCE, noble metal with defined shape and position is deposited on the top surface of Si. MaCE occurs when the metal-loaded Si is immersed in a HF−hydrogen peroxide (H_2O_2) solution; h^+ is generated by reduction of hydrogen peroxide (H_2O_2) under the catalysis of noble metals:



$$H_2O_2 + 2H^+ \xrightarrow{\text{noble metal}} 2H_2O + 2h^+ \quad (2)$$

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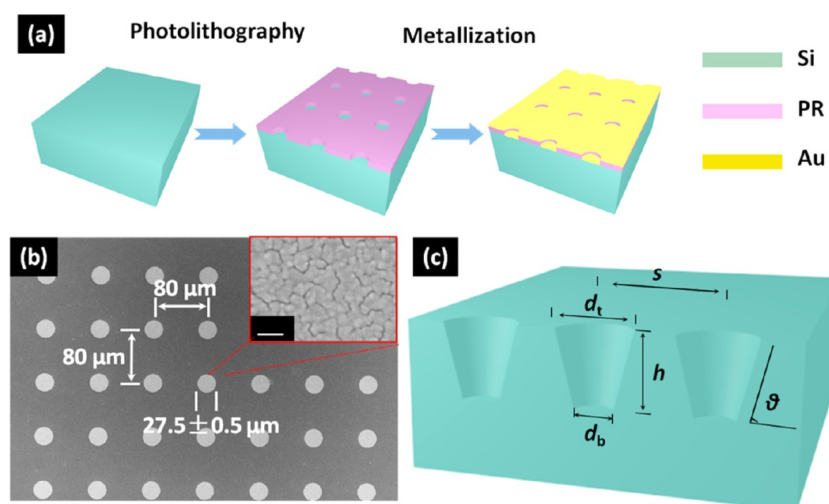

Figure 1. (a) Schematics of processing flow. The blocks in green, purple, and gold refer to Si substrate (Si), photoresist (PR), and Au catalysts (Au), respectively. (b) Top-view SEM image of Au patterns on silicon after lift-off of PR; (inset) morphology of Au pattern surface under high magnification (scale bar = 100 nm). (c) Schematic etching profile after MaCE and parameters used for describing the etching profile.

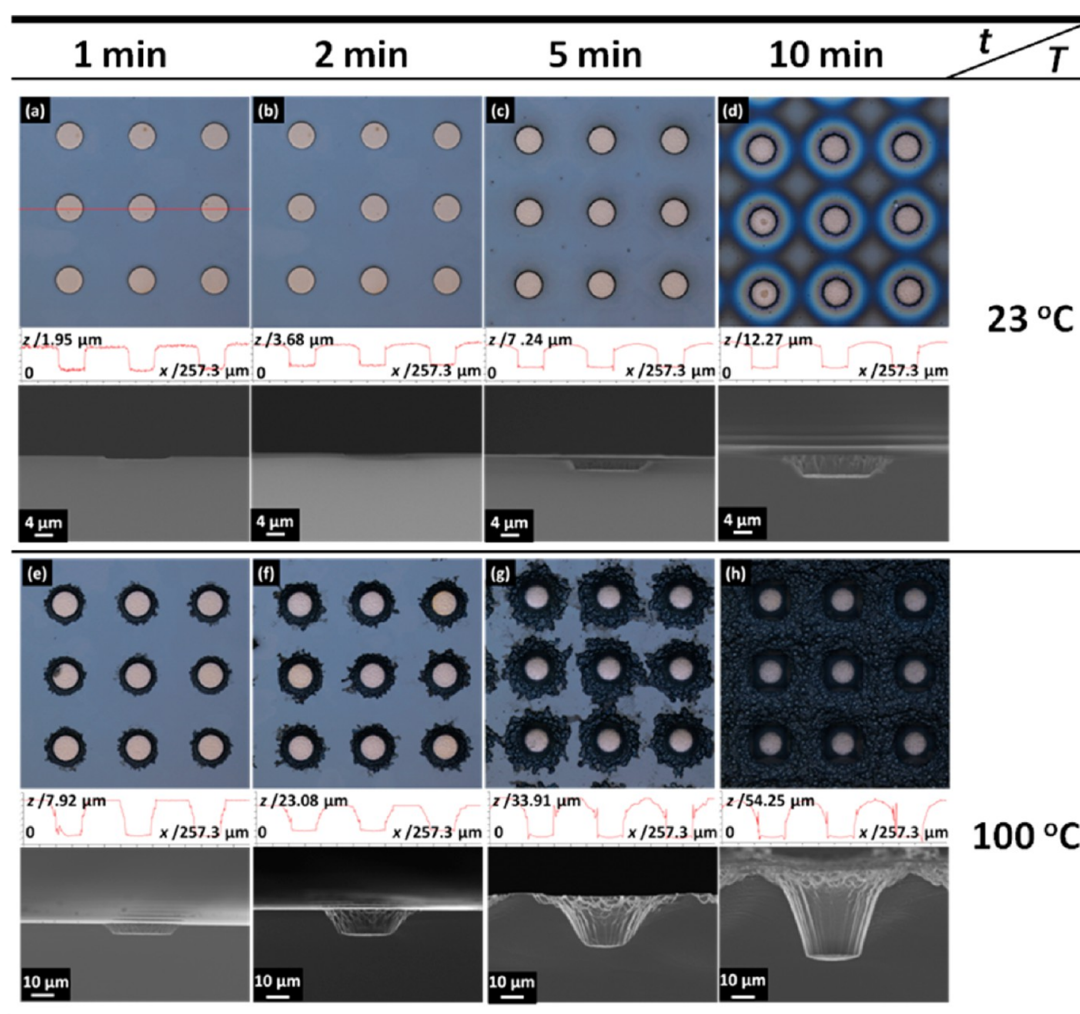

Figure 2. Etching profiles of 28 μm Au–Si(100) in $\rho(0.37)^{1.8}$ for (a) 1, (b) 2, (c) 5, and (d) 10 min at 23 °C and for (e) 1, (f) 2, (g) 5, and (h) 10 min at 100 °C. (Top) Top-view OCM images, (middle) optical cross sections, (bottom) and SEM cross sections are shown in each set of figures.

Then, h^+ induces the etching of Si adjacent to the metal catalysts following eq 1. The geometry of the etching profile can be controlled by the catalysts and etchant. Uniform silicon nanowires have been successfully fabricated by MaCE using mesh-shaped metal film.[18−21] However, BMS has been challenging for MaCE.[22] Recently, our group identified the

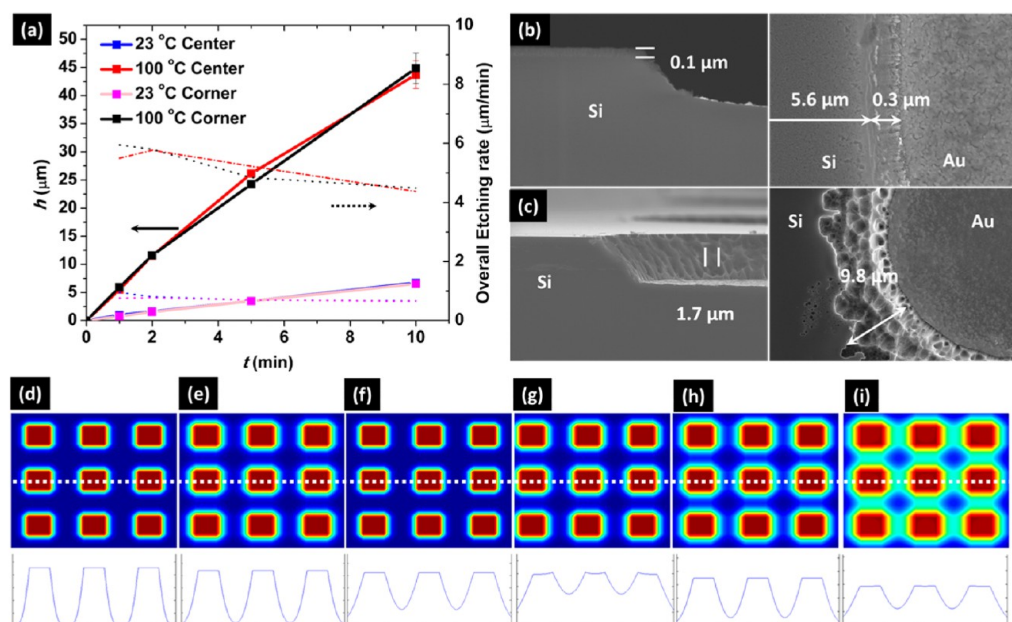

Figure 3. (a) Evolution of h (solid lines) and etching rate (dashed lines) versus etching time (t). (Left) High-magnification cross-sectional and (right) top-view SEM images of Au−Si boundary area after 1 min of etching at (b) 23 °C and (c) 100 °C. (d−i, top) Simulated 2D distribution of $c(h^+)$ in arbitrary unit (a.u.) corresponding to experiments shown in Figure 2a−f, respectively. The color bar indicates the relative value of $c(h^+)$ in the 2D plots with nominal dimension of 200 × 200 μm. (d−i, bottom) Corresponding distribution of c(h+) in a.u. along the dashed line.

transport of HF and h^+ to be the two critical processes for uniform MaCE. On the basis of this understanding, we established the uniform MaCE condition, in which a HF−H_2O_2 solution with a low HF-to-H_2O_2 concentration ratio (ρ) was used as the etchant to enable an electropolishing-favored h^+ transport; a nanoporous gold (Au) thin film was used as the catalyst to enable a through-catalyst transport of HF. A single uniform 2 μm wide trench was successfully fabricated under the uniform etching condition.[23] In this work, we investigate the MaCE of multiples microstructures with a broader range of shape and dimensions.

In the context mentioned above, we fabricated an array of circular Au catalysts with diameters of 27.5 ± 0.5 μm, spacing (the distance between the centers of two adjacent patterns) of 80 μm, and nominal thickness of 15 nm on (100)-oriented Boron-doped (resistivity, 1−10 Ω·cm) single crystalline Si wafers by photolithography and electron-beam evaporation (Figure 1a, referred to as the "28 μm Au−Si(100)" sample). Nanopores could be observed within the catalysts using a scanning electron microscope (SEM) (Figure 1b).The sample was cut into 1 cm^2 chips (referred to as the "chip" hereafter) for MaCE tests. The number of Au patterns on one chip is estimated to be 10^4. One drop (ca. 0.2 mL) of $\rho(0.22)^{0.9}$ HF−H_2O_2 aqueous solution was slowly dropped on the whole surface of 28 μm Au−Si(100) chip and kept for 1 min before the chip was fully immersed in 32 mL $\rho(0.37)^{1.8}$ HF−H_2O_2 aqueous solution (used in all following experiments unless specified). The name of the HF−H_2O_2 etchant is formatted as $\rho(x)^y$ to shows its composition, where x = [HF]/([H_2O_2] + [HF]) and y = [HF] ([HF] is the concentration of HF in moles per liter). The chip was etched with the photoresist on the top surface. Geometric parameters of the etching profile are defined in Figure 1c, including top diameter (d_t), bottom diameter (d_b), sidewall angle (θ), maximum etching depth (h) and spacing (s). After pre-etching by the $\rho(0.22)^{0.9}$ droplet, Au catalysts moved uniformly into Si substrate (Figure S2a, Supporting Information, while Si surrounding Au was also etched by with a width of 232 nm (Figure S2b, Supporting Information). Small etched pits were found right beneath the nanopores, both near the Au−Si boundary and under the center of Au patterns (Figure S2c,d, Supporting Information), indicating that HF was able to transport through the nanoporous Au catalysts. Also, we found the pre-etching step in the $\rho(0.22)^{0.9}$ etchant helped improve the reproducibility of experiments. The lower ρ value of pre-etching solution was found to facilitate a more stable etching at the initial stage. In a control experiment in which the chip was directly immersed in bulk $\rho(0.37)^{1.8}$ etchant without the pre-etching, some Au patterns were lifted off from Si substrate before any etching occurred. The pre-etching process is conducted in all the following experiments, and the time of pre-etching is excluded from the etching time mentioned below.

After immersion in the bulk $\rho(0.37)^{1.8}$ etchant, Au moved deeper into the Si chips. We studied the MaCE of 28 μm Au−Si(100) chips for 1 min, 2 min, 5 and 10 min at 23 and 100 °C. The etching profiles in each test are revealed by optical confocal microscopy (OCM) (top and middle images) and SEM (bottom images) in Figure 2. In the OCM images, Au and the Si between Au are shown in gold and blue. After etching, the catalysts moved vertically into the Si substrate and kept flat. The etching depth (h) and etching rate of each test are summarized in Figure 3a. The original data for plotting Figure 3a can be found in Tables S1 and S2 (Supporting Information). Etching depth (h) was measured from OCM cross sections of 9 adjacent etched holes in both center part (averaged to give h_{center}) and corner part (averaged to give h_{corner}) of the 1 cm^2 chips. The etching rate is calculated by dividing h by the corresponding etching time. After 10 min of MaCE, h_{center} reached 6.7 ± 0.1 μm at 23 °C and 43.7 ± 2.5 μm at 100 °C, while h_{corner} was 6.5 ± 0.2 μm at 23 °C and 44.9 ± 2.7 μm at 100 °C. Across the 10 min, the etching rate ranges were 0.95−0.67 μm/min at 23 °C and 5.50−4.37 μm/min at 100 °C. The

uniformity and speed of etching along the vertical direction at 100 °C is comparable to the commercial dry etching method.[24] The slight decrease of etching rate versus etching time may be due to the increasing difficulty of mass transport inside the etched holes.

In the above MaCE experiments, besides the vertical etching, significant etching also occurred in nonvertical directions. After 10 min of MaCE, the top surface of Si between Au patterns turned colorful at 23 °C (Figure 2d) and became completely black at 100 °C (Figure 2h), as can be observed in OCM images. Under magnified SEM images, these regions show a porous morphology. Actually, formation of the porous regions started from the first 1 min of MaCE, when the Si near Au−Si boundary was found completely removed by 300 nm in width (completely removed region, CRR) at 23 °C, and a porous layer expanded with a width of 5.6 μm beyond the CRR (Figure 3b); at 100 °C, the surface of CRR was decorated with much larger pores and extended 9.8 μm out of Au−Si boundary (Figure 3c). Apparently, the porous region and CRR are detrimental to electronic components, and thus, it is imperative to suppress the excessive etching before MaCE can be applied to any component fabrication.

Given that the etching of bare silicon by H_2O_2−HF solution is negligible,[25] we attribute the appearance of these regions to the electrochemical etching process (eq 1) induced by excessive h^+. In $\rho(0.37)^{1.8}$ etchant where $c(H_2O_2)$ is high, the amount of h^+ generated in eq 2 exceeds the amount that can be consumed by the etching of Si underneath the Au catalysts (i.e., the vertical etching). The excessive h^+ tends to diffuse to the sidewall and top surface of Si, which induces the nonvertical excessive etching in these regions (Figure 4a). Because both the vertical etching and the excessive etching follow the same process in eq 1, they both become faster at elevated temperature.[26] To further illustrate the origin of excessive etching, we simulated the distribution of accumulated h^+ concentration ($c(h^+)$) by a 2D constant source model.[23,27] The details of simulation can be found in the Supporting Information. Figure 3d−i shows the distribution of $c(h^+)$ plotted in 2D planes that contains 9 Au patterns (top images) and along 1D lines that intersect with 3 Au patterns (bottom images). Au patterns are set as the constant source of h^+. As visualized in both images, a significant amount of h^+ diffuses to the Si between Au ($c(h^+)_{Si}$) relative to that under the Au patterns ($c(h^+)_{Au}$) as the etching proceeds. At 23 °C, $c(h^+)_{Si}$ reaches ca. 60% of $c(h^+)_{Au}$ after 10 min; at 100 °C, $c(h^+)_{Si}$ reaches ca. 45% of $c(h^+)_{Au}$ only after 2 min. The evolution of $c(h^+)_{Si}$ in both cases is consistent with the expansion of porous region and CCR, which supports our assumption that excessive etching is induced by excessive h^+.

In this work, we demonstrate that the excessive etching can be controlled by using an external electric bias during MaCE process. We name the novel etching method as electric bias-attenuated MaCE (EMaCE). To maintain the high etching rate, all following experiments are done at 100 °C. On the basis of the above discussion, the excessive etching is supposed to originate from the excessive h^+. If a negative bias is applied from the back side of the chips, excessive h^+ will be drawn away from the sidewall and top surface to the back side of Si by electrostatic force, and the extent of excessive etching can be controlled by the strength of the bias (Figure 4b). The idea was realized by connecting the chip to the negative output terminal of a direct current electric power supply. To ensure good electrical contact between the chip and power supply, we

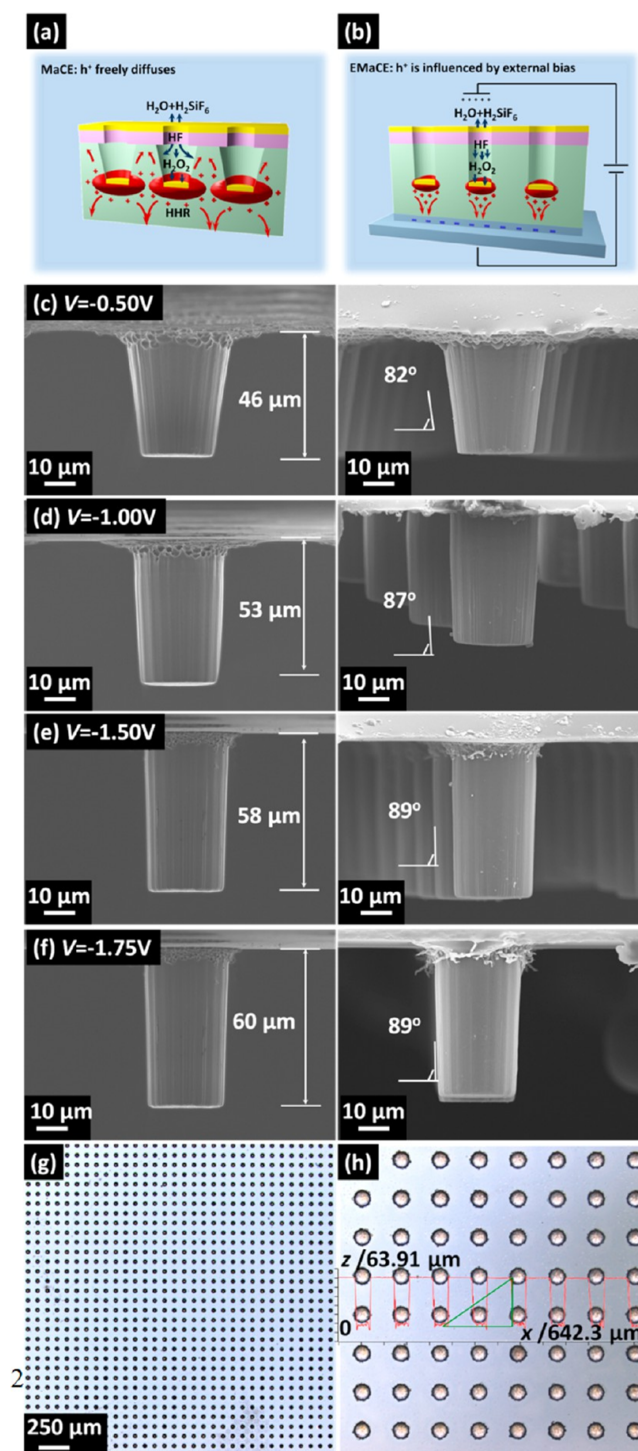

Figure 4. Schematics of charge transport in (a) MaCE and (b) EMaCE. Cross-sectional SEM images of the (left) chips and (right) polymer replica after EMaCE at (c) −0.50, (d) −1.00, (e) −1.50, and (f) −1.75 V for 10 min. (g) OCM image and (h) cross section of the etched chip in panel f.

mounted the chip on a gallium-wet copper foil that was wired to the power supply. The chip and copper foil were further packaged in a homemade carrier in which all surfaces were covered by polymer except the front surface of the chip (Figure S3, Supporting Information). The chip−copper−carrier assembly is referred as the working electrode. Meanwhile, a platinum (Pt) wire was connected to the positive terminal as

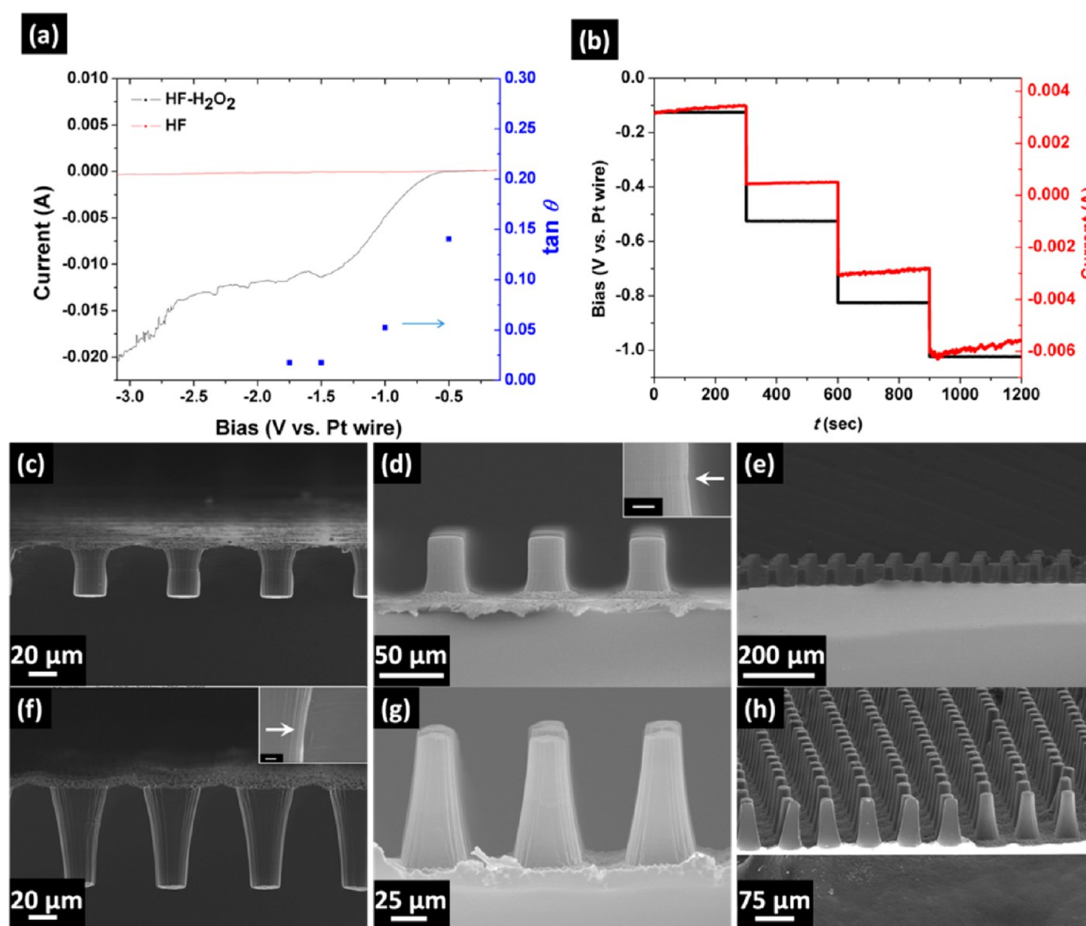

Figure 5. (a) Current-bias ($I-V$) curve of 28 μm Au–Si(100) in $\rho(0.37)^{1.8}$ etchant (black line) and $\rho(1)^{1.8}$ etchant (red line) in a continuous EMaCE experiment; h and θ of the etching results shown in Figure 4 c–f are also plotted. (b) Evolution of applied bias and measured current versus etching time in a stepwise EMaCE experiment. Cross-sectional SEM of (c) chips and (d and e) polymer replica etched under the conditions of the black line in panel a. Cross-sectional SEM of (f) chips and (g and h) polymer replica etched under the conditions of panel b.

the counter electrode. In EMaCE, both electrodes were immersed in the $HF-H_2O_2$ etchant, while a certain value of voltage (V) was set in the power supply so that the chip was negatively biased by V relative to the Pt wire (referred as "at $-V$"). The details of experimental setup and carrier fabrication are described in the Supporting Information. The first 30 s is included in the etching time mentioned below. After the 30 s of etching at no bias, d_t slightly increased to 29 μm. After EMaCE, we used polymer replica to reveal the true 3D geometry of the etching profile (see explanation in Figure S4, Supporting Information). The cross sections of the etched chips and corresponding polymer replica after EMaCE at −0.5, −1.0, −1.5, and −1.75 V for 10 min are shown in Figure 4c−f, respectively. Both cross sections consistently show a decrease of θ and an increase of h as the bias becomes more negative (referred to as an increase of bias). The results support our proposed mechanism that diffusion of excessive h^+ can be influenced by negative bias; as the strength of bias increases, more h^+ that tends to diffuse toward the top surface and sidewalls is driven toward the backside. In other words, the negative bias redistributes the $c(h^+)$ in 3D space so that excessive etching is suppressed and the vertical etching is enhanced. When the bias was increased to −1.75 V, the surface of Si between Au patterns keeps its original color and polished morphology (Figure 4g), and d_t remains 29 μm, indicating a complete suppression of excessive etching. Figure 4h shows the top-view OCM images and cross sections of the chip etched at −1.75 V. The h_{center} and h_{corner} are measured to be 59.8 ± 0.5 μm and 60.5 ± 0.5 μm, respectively. However, a much larger discrepancy was discovered between h_{center} and h_{corner} in EMaCE at −1.0 and −1.50 V (Figure S5, Supporting Information). The smaller discrepancy of h_{center} and h_{corner} found at −1.75 V is probably due to a complete suppression of excessive h^+ diffusion across the whole chip. The fact that excessive etching can be experimentally suppressed by negative bias further supports the assumption that the excessive etching is caused by excessive h^+.

To further illustrate the proposed mechanism of EMaCE, we replaced the constant bias by a variable bias that continuously increased from −0.10 to −3.10 V at 5 mV/s (referred as continuous EMaCE experiment). The current-bias ($I-V$) curve of the continuous EMaCE experiment is shown as the black line in Figure 5a. The sign of current is defined as negative, meaning that h^+ is flowing away from the chip and electrons are injected into the chip. Because the Si substrate is p-type, the contact between the back side of Si and the copper foil can be treated as a forward-biased Schottky contact. The nonlinear increase of current versus bias beyond the onset of ca. −0.6 V is characteristic for forward-biased Schottky contact. After the bias exceeds −1.5 V, the evolution of current became unstable, which may be due to the slow depletion of excessive h^+. In contrast, when the same experiment was done in a $\rho(1)^{1.8}$

etchant (i.e., etchant without H_2O_2), the current stays negligibly low across the whole etching experiment (red line, Figure 5a). Actually, Au catalysts hardly etched into the substrate in $\rho(1)^{1.8}$, and only some pores (<100 nm diameter) propagated along the family of ⟨100⟩ crystalline orientation around the Au (Figure S6, Supporting Information). The control experiment indicates that catalyzed reduction of H_2O_2 is the source of the current in EMaCE (black line Figure 4a), and the charge carriers of the current mainly consist of excessive h^+. Thus, EMaCE is essentially different from traditional electrochemical etching[28] in which h^+ is injected from an external power supply. We also plot the value of tan θ from Figure 4c−f against the bias as blue dots in Figure 5a, which shows a decreasing trend similar to that of current. Because tan θ approximately equals to $2h/(d_t - d_b)$, tan θ can roughly represent the ratio of the vertical etching rate to the excessive etching rate. The similarity between the trends of $I-V$ and $\tan(\theta - V)$ indicates that the extent of excessive etching suppression can be related to the amount of h^+ that are drawn to the back side. Further, we did an EMaCE experiment where the applied bias varied versus etching time in a stepwise manner (referred to as stepwise EMaCE). The evolution of applied bias and measured current versus the etching time are shown in Figure 5b. The etching process can be divided into four stages. In each stage, the bias stayed at a constant value for 300 s. The transition time of the bias and current between two stages are both less than 1 s. The current changed and stabilized itself after the bias was altered to a new value with delay time less than 1 s. The slight increase of current in each stage may be caused by the geometric evolution of the etching profile. The etching result of continuous EMaCE and stepwise EMaCE are shown in Figure 5c−e and f−h, respectively. In continuous EMaCE, the sidewall angle increased as the Au etched deeper; the sidewall angle become 90° around 20 μm below the top surface. In stepwise EMaCE, the sidewall angle increased stepwise. In both cases, some discontinuity on the smooth sidewall can be observed (Figure 5d,f, insets). These sharp turns show the geometric response of etching profile to the attenuation of applied bias.[29,30] Also, the etching profiles are uniform across the whole chips, as illustrated by the low-magnification SEM images of polymer replica (Figure 5e,h). The success of continuous EMaCE and stepwise EMaCE demonstrates that both the lateral and the vertical geometry of the etching profile can be controlled in a real-time manner by the facile attenuation of bias over etching time.

To investigate capability of high-speed etching by EMaCE, we performed EMaCE in $\rho(0.55)^{3.6}$ etchant. After 10 min of etching, the catalysts penetrated 113 μm into the silicon substrate with a sidewall angle >89° (Figure 6a,b). When viewed under SEM with high magnification, the sidewall shows a roughness well below 50 nm (Figure 6f). The low sidewall roughness (<50 nm) at high etching speed (>10 μm/min) makes the etched holes ideal candidates for high performance through silicon vias. In contrast, in dry etching, the sidewall roughness is usually compromised at an etching rate higher than 5 μm/min.[24] Further increasing the ρ value of the etchant may cause the catalysts to break. As shown in Figure S7 (Supporting Information), after etching in $\rho(0.65)^{5.2}$ at −1.75 V for 10 min, Au catalysts broke into separate particles. Randomly aligned pores were formed on both the top surface and the bottom of the etched holes (Figure S7a,b, Supporting Information), because a porous silicon-formation h^+ transport was enabled in the high-ρ etchant.[23] Further, we investigated

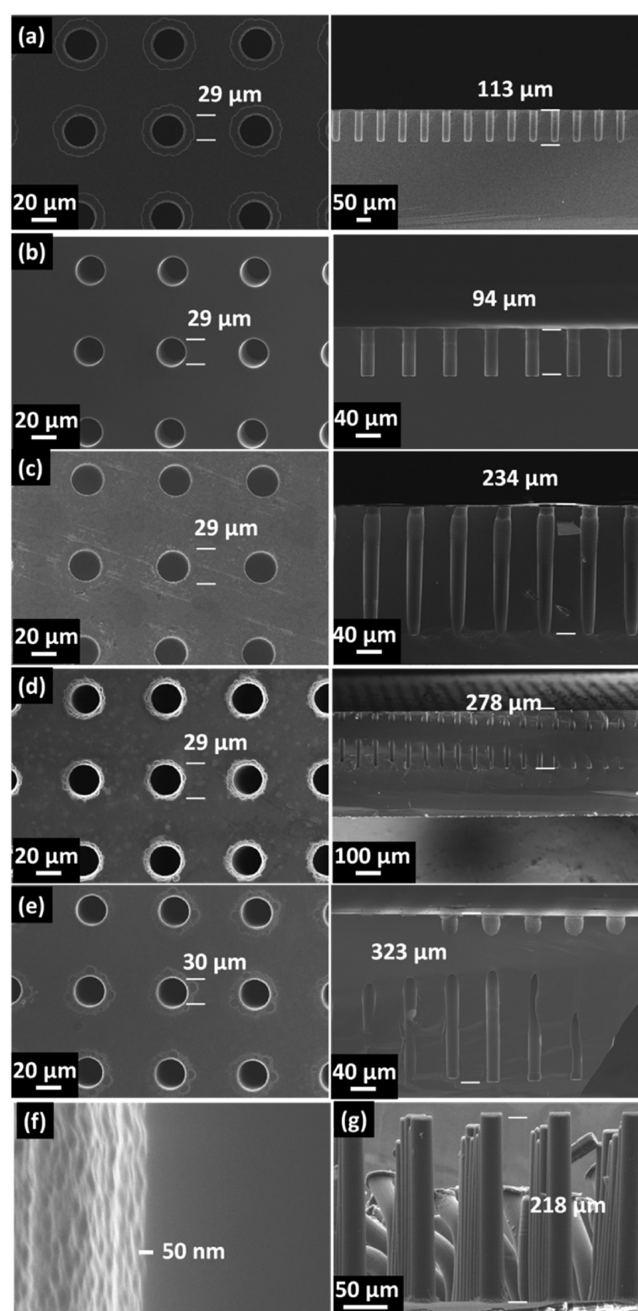

Figure 6. (Left) Top-view and (right) cross-sectional of the chips etched at −1.75 V for (a) 10 min in $\rho(0.37)^{1.8}$, (b) 25, (c) 60, (d) 90, and (e) 120 min. (f) Sidewall of etched holes in panel a with high magnification. (g) Polymer replica of chip in panel d.

the capability of EMaCE in etching structures with high aspect ratio. Figure 6b−d shows the chips after EMaCE in $\rho(0.37)^{1.8}$ at −1.75 V for 25 min, 60 min, 90 and 120 min. In each test, the etchant was agitated by a stir bar at 400 rpm after 10 min of EMaCE; d_t remained 29 μm in each test; and h was measured each time from cross sections of the etched chips, which are 94, 235, 278, and 323 μm, respectively. The low-magnification images of the chips after 25 min of etching show good uniformity across the whole chips (Figure S8a,b, Supporting Information). After an etching time of 120 min, the vertical etching direction was still preferred. The Au catalyst maintained its integrity without breaking, and the sidewall roughness remained as low as that shown in Figure 6f. We also tried to use

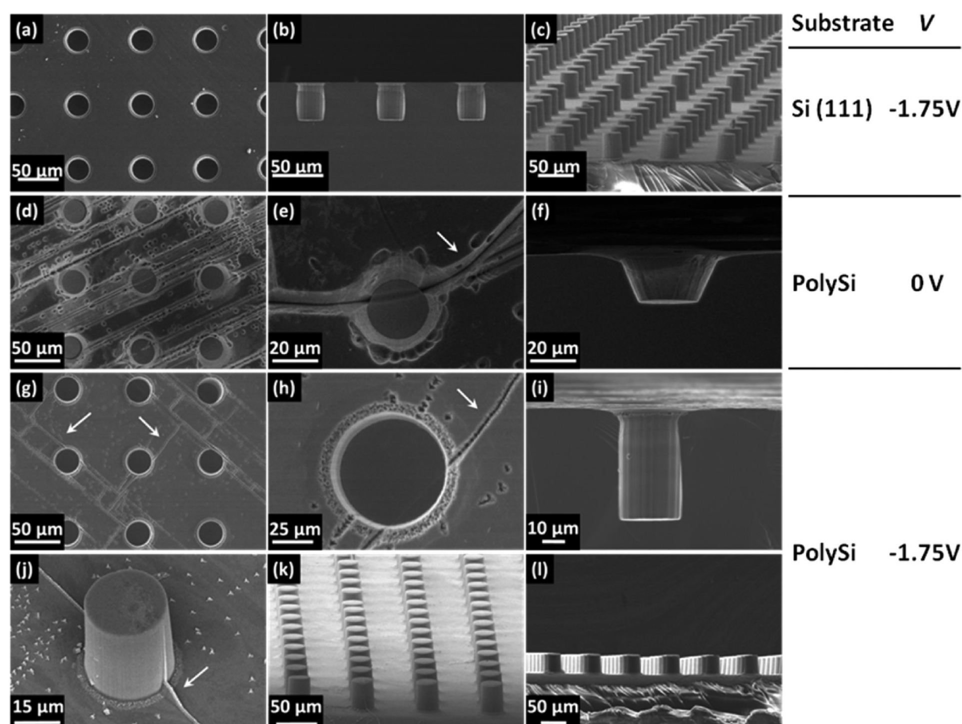

Figure 7. (a) Top-view and (b) cross-sectional SEM images of a 29 μm Au−Si(111) chip after MaCE at −1.75 V and (c) corresponding replica. (d and e) Top-view and (f) cross-sectional SEM images of a 29 μm Au-polySi chip after MaCE. (g and h) Top-view and (i) cross-sectional SEM images of a 29 μm Au-polySi chip after MaCE at −1.75 V. (j−l) Corresponding replicas.

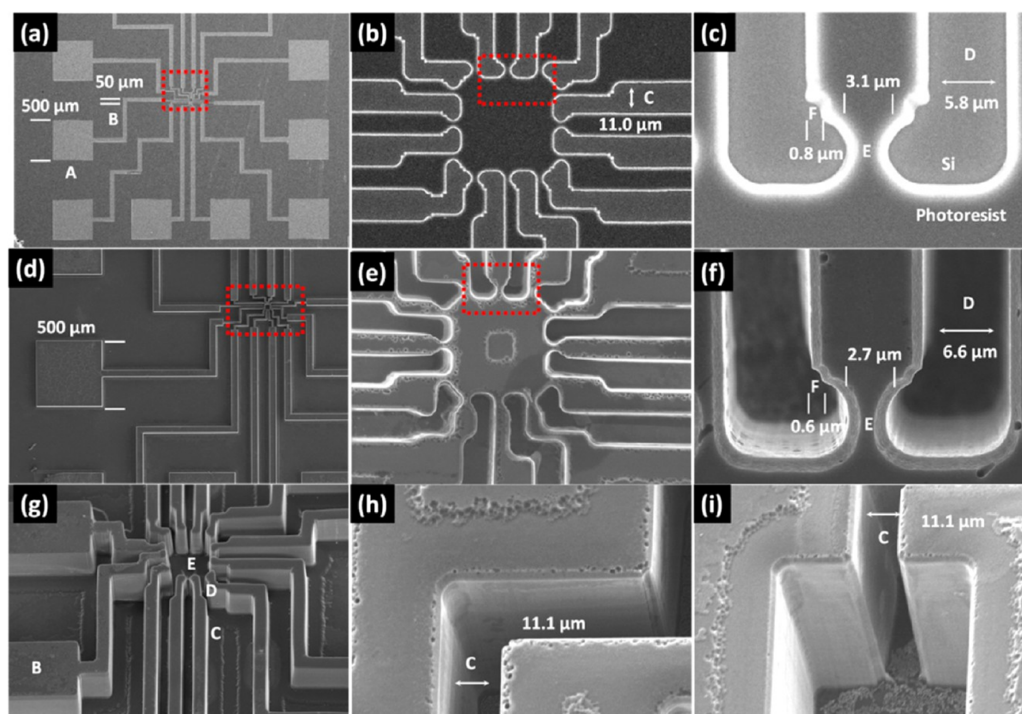

Figure 8. (a−c) Pattern of a complex feature after photolithography on Si(100) chip; (e−h) the chip after EMaCE at −2.00 V for 10 min; and (d and g) the corresponding replicas.

polymer replica to reveal the 3D geometry of these high-aspect-ratio structures. However, because of the limited mechanical property of epoxy replica, only straight polymer replica with the height of 218 μm was found. Some replica with a height of 270 μm can also be found while tilting from the vertical direction (Figure S8c, Supporting Information). It should be noted that after etching for 120 min at −1.75 V, the photoresist stayed in close contact with the top surface of silicon substrate (Figure S8d, Supporting Information). In contrast, the top surface was significantly etched, and a gap appeared after 20 min of MaCE at no bias (Figure S8e, Supporting Information) and finally caused the delaminating of photoresist. The results shown in

Figure 6b−e demonstrate that EMaCE is capable of producing microstructures deeper than 300 μm with an aspect ratio greater than 10:1 while completely suppresses the excessive etching over the etching long time.

To extend the range of application, we applied the established EMaCE method to the BMS of (111)-oriented Si substrate and polycrystalline Si (polySi) substrate. Figure 7a−c shows the top-view and cross-sectional SEM images of a 29 μm Au−Si(111) chip after EMaCE for 10 min at −1.75 V and the corresponding replica. Uniform vertical holes can be found across the whole chip. For polySi substrate, we first studied the etching behavior at no bias (Figure 7d−f). After etching for 10 min, Au catalysts moved vertically into the substrate. However, a considerable amount of grooves and pits were found on the Si between Au (Figure 7d). It has long been known that chemical etching of Si is preferable along the defects of Si substrates.[31]Thus, the grooves were probably formed by the excessive etching of the boundary between two adjacent Si crystal grains. At higher magnification, some grooves were found to penetrate below the Au catalysts, indicating that the excessive etching of grain boundary even exceeded the MaCE process (indicated by the white arrow Figure 7e). Also, the sidewall of the etched holes tapered like those shown in Figure 2. In contrast, when a −1.75 V bias was applied, both the groove formation and sidewall tapering were suppressed (Figure 7g−i). Although some shallow grooves were still observable, the grooves only penetrated into the very top layer of Si substrates, as revealed from the etched chip (Figure 7h) and its corresponding replica (Figure 7j). Also, etching in the vertical direction was significantly enhanced by the bias (Figure 7i) compared to that at not bias (Figure 7f). The SEM of polymer replica in low magnification (Figure 7k,l) shows that the vertical etching was preferred across the chip, and all the etched holes bear high geometric uniformity. The crystalline orientation-independent etching behavior is highly desirable for BMS on broader range of substrates.

Finally, we tested the BMS of complex features by EMaCE. Figure 8a−c shows the original pattern of a complex feature after photolithography. Five sets of subunits with critical dimensions of (A) 500, (B) 50, (C) 11.7, (D) 5.8, (E) 3.1, and (F) 0.8 μm can be observed in the images with increasing magnification (Figure 8). We increased the bias to −2.00 V because a larger amount of excessive h^+ was produced by the larger area of Au catalysts. After 10 min of EMaCE, Au catalysts on all units etched uniformly and vertically into the Si substrate, as shown in the polymer replica (Figure 8d,g). The values of d_t and d_b were measured from the etched chips (Figure 8e,f) and corresponding polymer replica (Figure 8g), respectively. The values are listed in Table 1. The variance between d_t and d_b of each subunit is less than 1 μm, both of which have a variance less than 1 μm to their origin dimensions (d_{orig}). Besides the accuracy of dimensions, EMaCE also possesses the fidelity in transferring the shape of original features, as found in the sharp corners (Figure 8h) and interconnections between features B and C (Figure 8i).

Table 1. Dimensions of Subunits C−F Shown in Figure 8 before and after EMaCE

feature ID	C	D	E	F
d_{orig}(μm)	11.0	5.8	3.1	0.8
d_t(μm)	11.1	6.6	2.7	0.6
d_b(μm)	10.2	5.0	2.7	0.8

■ CONCLUSION

In conclusion, a novel silicon etching method, named electric bias-attenuated metal-assisted chemical etching (EMaCE), is established on the basis of the uniform MaCE condition. A negative electric bias was applied from the back side of Si substrate during MaCE process to solve the issue of excessive etching found in traditional MaCE process. Over 10 000 vertical holes with diameter of 28 μm were successfully fabricated on a 1 cm^2 chips with high speed, high aspect ratio, and low sidewall roughness. By programming the variation of bias versus etching time, the 3D geometry of the etching profile can be attenuated in real time. Etching of vertical holes was also realized by EMaCE on Si (111) and polySi substrate. Complex features with lateral dimensions of 0.8 μm-500 μm were also fabricated with high geometric accuracy. The established EMaCE is not only readily applicable for manufacturing TSVs in large scale with low cost, but it is also available for MEMS devices with complex lateral geometry. Also, EMaCE provides a viable solution for direct deep etching of polycrystalline silicon, which has been challenging so far. Further, EMaCE with variable bias is promising to create novel micro- and nanostructures with arbitrarily defined 3D complexity that spur the leap in microelectronics packaging, MEMS, photonic devices, and so on.

■ EXPERIMENTAL SECTION

Substrate Preparation. Boron-doped (100)-, (111)-oriented single crystalline silicon wafers (1−10 Ω·cm) and polycrystalline silicon wafers (boron-doped, 1−10 Ω·cm) with one side polished were purchased from University Wafer (Boston, MA). In a Class 10 cleanroom, the wafers were cleaned in Piranha solution (1:3 volume ratio of H_2O_2 (30 wt %) and H_2SO_4 (96 wt %))at 120 °C for 10 min, and then dipped in 1% w/w aqueous HF solution to remove the oxide layer. The cleaned wafers were dried in N_2. For photolithography, a 1.6 μm-thick layer of negative photoresist NR9−1500PY (Futurrex, Inc., Franklin, NJ) was spin cast on the front (polished) side of the cleaned wafer and exposed in a mask aligner (Karl Suss MA6) by 365 nm UV light with a dosage of 190 mJ/cm^2. The exposed wafer was developed by immersion in Resist Developer RD6 (Futurrex, Inc., Franklin, NJ). All the wafers with patterned resist are treated with oxygen plasma (RF power: 22 W) in an RIE tool (Plasma Therm, Inc.) to remove any polymer residue on exposed areas and make the silicon surface terminated by oxygen (Si−O). Au catalysts were deposited on the front side by an electron beam evaporator at a rate of 0.5 Å/s in a vacuum atmosphere of 3×10^{-6} Torr (CVC Product, Inc.). Then, 10 nm thick titanium and 200 nm thick copper were deposited on the back side of the wafers using the same method. In this report, the thickness refers to the nominal value measured by an in situ monitor (Maxtek Sensor Crystal Gold 6 MHz 74016−1139 P/N 103220, Inficon), unless specified.

Etching and Characterization. The wafers were cut into 1 cm^2 chips and mounted on homemade carriers before etching. Briefly, the carriers were made by spreading a layer of copper foil (0.127 mm thick, Alfa Aesar) on a 1.5 × 2.0 cm glass slide. A polymer-coated copper wire (0.50 mm conductor diameter, R24BLK-0100, OK Industries) was soldered on one corner of the copper foil. The edge of the carrier was sealed by epoxy precursor and cured at 150 °C for 1 h in an atmospheric oven. The epoxy precursor was prepared by mixing 17 g of EPON Resin 862, (Hexion Special Chemicals, Inc.), 20 g of Lindride 52D (Lindau Chemicals) and one drop of 2-ethyl-4-methyl-1*H*-Imidazole-1-propanenitrile (Aldrich) as catalyst. After sealed in the epoxy, the chip was mounted on the copper foil, which had been wetted by liquid gallium for good electric contact. The test vehicle was

further sealed by polyimide tape to make only the front sides of chips exposed (Figure S3, Supporting Information). To prepare the etchant, HF (48−52 wt % in H_2O), H_2O_2 (30 wt % in H_2O, Anachemia Chemicals, LLC) and deionized water (DI water, resistivity ~18.2 MΩ) were directly mixed without further processing. DI water was produced by a Thermo Scientific Barnstead Smart2Pure water purification system. The total volume of the etchant was fixed to 32 mL. The etching was conducted by gently immersing the test vehicle in the etchant solution in a loosely capped transparent polyethylene (PE) tube (VWR International, Suwanee, GA) for a certain amount of time. The PE tube with etchant was preheated in a silicone oil bath with controlled temperature on a hot plate (VWR International, Radnor, PA) for 20 min before etching and kept immersed in the bath until etching was finished. After being etched, the chips were taken off the carriers and cleaned by Piranha solution described above. Note: $HF-H_2O_2$ mixture and Piranha solution is highly corrosive, thus the etching and cleaning were done in a well-ventilated fume hood with proper personal protection equipment. A constant bias was generated by a power supply (Farnell PSD 3510A). The variable voltage was produced and recorded by a potentiostat (Princeton Applied Research, VersaSTAT MC). The bias was applied 30 s after the chip was immersed in the etchant to stabilize the Au catalysts. The polymer replica was fabricated by dipping the epoxy precursor on the front side of cleaned chips after etching and cured at 150 °C in a vacuum oven for 1 h. The replica is isolated by completely removal of silicon in the mixture of HNO_3 (70 wt %) and HF (49 wt %) with the volume ratio of 1:6 within 10 min at room temperature. The polymer replica was coated by Au (less than 20 nm thick) for SEM imaging in a DC-sputter (Denton DeskII). SEM images were taken from Zeiss LEO 1550 thermally assisted field emission (TFE) SEM or Hitachi SU8010 SEM operating at 10 keV with a working distance between 2 and 7 mm. Optical confocal microscope image and cross sections were obtained from Olympus LEXT OLS4000 laser confocal microscope. The depth of pre-etching step was measured by Tencor P15 Profilometer using stylus. Matlab 7.0 software was used for modeling h^+ concentration.

■ ASSOCIATED CONTENT

Supporting Information

SEM images and details of h+ simulation. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

L.L. conducted the experiments and analyzed the data. X.Z. did the simulation of h^+ concentration. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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